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SYSTEM AND METHOD FOR PROVIDING IMPROVED TRENCH ISOLATION OF SEMICONDUCTOR DEVICES

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SYSTEM AND METHOD FOR PROVIDING IMPROVED TRENCH ISOLATION OF SEMICONDUCTOR DEVICES

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is generally directed to manufacturing technology for semiconductor devices and, in particular, to a system and method for providing improved trench isolation of semiconductor devices.

BACKGROUND OF THE INVENTION

[0002] Trench isolation is commonly used in semiconductor integrated circuits. Trench isolation provides improved isolation performance with regard to leakage and breakdown voltage. Trench isolation also takes less space than other methods such as junction isolation or LOCOS (Local Oxidation of Silicon).

[0003] The desire to save space causes trenches to be etched with high aspect ratios. A high aspect ratio for a trench means that the trench has a large vertical depth relative to the lateral width of the trench. Trenches that have a high aspect ratio are often filled with polysilicon that is deposited by low pressure chemical vapor deposition (LPCVD). LPCVD polysilicon is highly conformal and is able to coat the walls and bottom of a trench far from the surface of a wafer.

[0004] Polysilicon has the added advantage that it has the same thermal expansion coefficient as the surrounding monocrystalline silicon in which the semiconductor device is built. However, because polysilicon is not an insulator, the polysilicon must be separated from the adjacent monocrystalline silicon areas on either side of the trench with an insulator. The insulator that is most often used is a thermally grown silicon dioxide layer.

[0005] During subsequent processing steps the silicon dioxide layer can cause problems. One problem is that the silicon dioxide layer can be attacked during wafer etching and precleaning. This may cause portions of the silicon dioxide layer to be eroded. Erosion of the silicon dioxide layer can leave a gap between a monocrystalline silicon portion and an adjacent polysilicon portion. The gap can trap undesirable materials, thereby compromising the isolation properties of the trench and causing the semiconductor device to fail.

[0006] Another problem is that the silicon dioxide layer provides a diffusion conduit for oxidizing species (e.g., oxygen or steam) during subsequent thermal processing. This causes oxidation along the lateral seam on both sides of the polysilicon of the trench structure as well as on the adjacent walls of monocrystalline silicon. Because silicon dioxide occupies approximately twice as much space as the space of silicon that it

consumes, the volume of material in the oxidized region of the trench expands substantially. This expansion creates stresses that cause defects (e.g., cracks) in the monocrystalline silicon areas. These defects can lead to leakage within the semiconductor device that the trench is designed to isolate. It is possible that the defects can even lead to the failure of the semiconductor device.

[0007] Therefore, there is a need in the art for a system and method for providing improved trench isolation for semiconductor devices in an integrated circuit. There is a need in the art for a system and method for manufacturing an isolation trench that does not expose the seams of polysilicon portions and adjacent monocrystalline silicon portions to subsequent etching and oxidation.

SUMMARY OF THE INVENTION

[0008] To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide a system and method for providing improved trench isolation of semiconductor devices.

[0009] In one advantageous embodiment of the present invention a trench isolation structure is constructed in the following manner. First an underlying monocrystalline silicon substrate layer is provided. Then a thick silicon dioxide layer is applied to the top of the monocrystalline silicon substrate layer. Then a layer of photoresist material is then applied on top of the silicon dioxide layer. Then the photoresist is selectively exposed and developed from the trench areas. Then portions of the silicon dioxide layer are etched in the trench areas.

[0010] Then the photoresist material is removed and a silicon trench etch procedure is applied to etch trenches in the monocrystalline silicon substrate layer. Then portions of the overlying silicon dioxide layer are etched away to pull the silicon dioxide layer back from the edges of the trenches. Then a silicon dioxide liner is grown on the monocrystalline silicon substrate layer. The silicon dioxide liner covers the walls and bottom of the trenches and the horizontal surfaces of the monocrystalline silicon substrate layer that are exposed at the edges of the trenches.

[0011] Then a layer of polysilicon is deposited using a low pressure chemical vapor deposition (LPCVD) process. The polysilicon material fills the trenches and covers the silicon dioxide layer that overlies the monocrystalline silicon substrate layer. Then a polysilicon etchback process is performed to etch away the top layer of the polysilicon material.

[0012] The polysilicon etchback process leaves a portion of polysilicon material on top of each polysilicon filled trench. The portion of polysilicon material that is located over the top of each polysilicon filled trench extends laterally over the edges of the isolation trench in a shape that suggests the form of a nailhead. For this reason the portion of polysilicon material that is located over the top of each polysilicon filled trench is referred to as a polysilicon nailhead.

[0013] The initial height of silicon dioxide layer and the overetch height of the polysilicon material are optimized to establish an appropriate height for the polysilicon nailhead. The height of polysilicon nailhead must be sufficient for the polysilicon nailhead to survive subsequent etches and oxidations. Then the silicon dioxide layer is stripped away leaving the polysilicon nailheads exposed above the surface of the monocrystalline silicon substrate layer.

[0014] The polysilicon nailhead structure protects the silicon dioxide liner in the trenches. That is, during subsequent oxidations the silicon dioxide liner that is located between the polysilicon material in the trenches and the surrounding monocrystalline silicon substrate layer is protected. Subsequent oxidation processes can not reach the protected silicon dioxide liner. There will be no increase in volume in the silicon dioxide liner because the oxidized polysilicon nailhead can expand laterally and vertically. Therefore, there will be no stress due to volume increase of the silicon dioxide liner. The absence of stress means that there will be no defects in the surrounding monocrystalline silicon substrate layer.

[0015] It is an object of the present invention to provide a system and method for providing improved trench isolation of semiconductor devices.

[0016] It is also an object of the present invention to provide a system and method for manufacturing an isolation trench structure in a semiconductor device that protects a silicon dioxide liner in an isolation trench.

[0017] It is yet another object of the present invention to provide a system and method for forming a portion of a polysilicon isolation trench fill material that extends laterally over the edges of an isolation trench.

[0018] It is still another object of the present invention to provide a system and method for forming a portion of a polysilicon isolation trench fill material in the form of a polysilicon nailhead structure.

[0019] The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

[0020] Before undertaking the Detailed Description of the Invention below, it may be advantageous to set forth definitions of certain words and phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be

included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, those of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior uses, as well as future uses, of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] For a more complete understanding of the present invention and its advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, in which like reference numerals represent like parts:

[0022] FIGURES 1 through 11 illustrate successive stages in the construction of two prior art isolation trench structures;

[0023] FIGURES 12 and 13 illustrate problems that may be encountered with prior art isolation trench structures;

[0024] FIGURES 14 through 26 illustrate successive stages in the construction of two isolation trench structures in accordance with the principles of the present invention;

[0025] FIGURE 27 illustrates a flow chart showing the steps of a first portion of an advantageous embodiment of the method of the present invention; and

[0026] FIGURE 28 illustrates a flow chart showing the steps of a second portion of an advantageous embodiment of the method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0027] FIGURES 1 through 28, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any type of suitably arranged semiconductor device.

[0028] FIGURE 1 illustrates a first stage in the construction of a prior art isolation trench structure 100. The construction of isolation trench structure 100 begins by providing a monocrystalline silicon substrate layer 110. As shown in FIGURE 2, a thick silicon dioxide layer 210 is applied to the top of the monocrystalline silicon substrate layer 110. This is done because a silicon trench etch procedure (to be subsequently performed) attacks photoresist much faster than oxide, and because a top oxide layer during a silicon trench etch procedure enables the tapering of the trench from top to bottom.

[0029] To simplify the drawings the reference numerals from previous drawings will sometimes not be repeated for structures that have already been identified.

[0030] A layer of photoresist 310 is then applied on top of the silicon dioxide layer 210. The result of this step is shown in

FIGURE 3. Then the photoresist 310 is selectively exposed and developed from the trench area. The result of this step is shown in FIGURE 4. Then portions of the silicon dioxide layer 210 are etched anisotropically in the trench areas. Photoresist 310 protects the silicon dioxide 210 that underlies the photoresist 310. The result of this step is shown in FIGURE 5.

[0031] Usually the photoresist 310 is removed before the silicon trench etch procedure is applied. The result of removing the photoresist 310 is shown in FIGURE 6. If the photoresist 310 is not removed at this stage then it is removed after the silicon trench etch procedure is performed and before further processing occurs.

[0032] Then the silicon trench etch procedure is performed. The result of performing the silicon trench etch procedure is shown in FIGURE 7. The silicon trench etch procedure will also etch the photoresist 310 if the photoresist 310 is still present on top of the silicon dioxide layer 210. The silicon trench etch procedure will also etch the silicon dioxide layer 210 if the photoresist 310 has already been removed.

[0033] Then the silicon dioxide layer 210 is removed. The result of performing this step is shown in FIGURE 8. Then a silicon dioxide liner 910 is grown on the monocrystalline silicon substrate layer 110 in which the two trenches have been etched. The result of

performing this step is shown in FIGURE 9. Then a layer of polysilicon 1010 is deposited using a low pressure chemical vapor deposition (LPCVD) process. The result of performing the LPCVD process to deposit the polysilicon 1010 is shown in FIGURE 10. The two trenches are filled with polysilicon material 1010.

[0034] Then a polysilicon etchback process is performed to etch away the top layer of the polysilicon 1010. The result of performing the polysilicon etchback process is shown in FIGURE 11.

[0035] FIGURE 12 illustrates one of the problems with prior art isolation trenches. Subsequent cleans and oxide etches may remove portions of the silicon dioxide liner 910 from the interface between monocrystalline silicon substrate layer 110 and the polysilicon material 1010 in the trenches. Removal of the silicon dioxide liner 910 may create gaps 1210 such as those shown in FIGURE 12. The gaps 1210 between the monocrystalline silicon substrate layer 110 and the polysilicon material 1010 compromise the isolation properties of the trenches and may cause a semiconductor device located between the trenches to fail. The gaps 1210 also create likely locations for incomplete etch and trapping sites for contamination.

[0036] FIGURE 13 illustrates another problem with the structure of prior art isolation trenches. The silicon dioxide layer 910 provides a diffusion conduit for oxidizing species (e.g., oxygen or

steam) during subsequent thermal processing. This causes oxidation along the lateral seam between the polysilicon material 1010 of the trench structure and the adjacent walls of the monocrystalline silicon substrate layer 110. Because silicon dioxide occupies approximately twice as much space as the space of silicon that it consumes, the volume of material in the oxidized region of the trench expands substantially.

[0037] The expanded volume of the silicon dioxide is represented in FIGURE 13 as triangular portions. The expansion of the silicon dioxide creates stresses that cause defects (e.g., cracks) in the monocrystalline silicon substrate 110 layer. These defects can lead to leakage within the semiconductor device (not shown) that the trenches are designed to isolate. It is possible that the defects can even lead to the failure of the semiconductor device.

[0038] The problems that occur with prior art isolation trenches do not exist in isolation trenches that are constructed in accordance with the principles of the present invention. An advantageous embodiment of a method of constructing isolation trenches of the present invention will now be described.

[0039] FIGURE 14 illustrates a first stage in the construction of an isolation trench structure 1400 of the present invention. The construction of isolation trench structure 1400 begins by providing a monocrystalline silicon substrate layer 1410. As shown

in FIGURE 15, a thick silicon dioxide layer 1510 is applied to the top of the monocrystalline silicon substrate layer 1410. This is done because a silicon trench etch procedure (to be subsequently performed) attacks photoresist much faster than oxide, and because a top oxide layer during a silicon trench etch procedure enables the tapering of the trench from top to bottom. In addition, the thickness of the silicon dioxide layer 1510 is optimized to control the height of a raised portion of polysilicon that will be subsequently added.

[0040] A layer of photoresist 1610 is then applied on top of the silicon dioxide layer 1510. The result of this step is shown in FIGURE 16. Then the photoresist 1610 is selectively exposed and developed from the trench area. The result of this step is shown in FIGURE 17. Then portions of the silicon dioxide layer 1510 are etched anisotropically in the trench areas. Photoresist 1610 protects the silicon dioxide 1510 that underlies the photoresist 1610. The result of this step is shown in FIGURE 18.

[0041] Usually the photoresist 1610 is removed before the silicon trench etch procedure is applied. The result of removing the photoresist 1610 is shown in FIGURE 19. If the photoresist 1610 is not removed at this stage then it is removed after the silicon trench etch procedure is performed and before further processing occurs.

[0042] Then the silicon trench etch procedure is performed. The result of performing the silicon trench etch procedure is shown in FIGURE 20. The silicon trench etch procedure will also etch the photoresist 1610 if the photoresist 1610 is still present on top of the silicon dioxide layer 1510. The silicon trench etch procedure will also etch the silicon dioxide layer 1510 if the photoresist 1610 has already been removed.

[0043] Then portions of silicon dioxide layer 1510 are etched away as shown in FIGURE 21. The portion of silicon dioxide layer 1510 are etched isotropically. The height of the remaining silicon dioxide layer 1510 and the distance that the silicon dioxide layer 1510 is pulled back from the trench edge are optimized based on subsequent processing to be performed.

[0044] Then a silicon dioxide liner 2210 is grown on the monocrystalline silicon substrate layer 1410 in which the two trenches have been etched. The silicon dioxide liner 2210 covers the walls and bottom of the trenches. The silicon dioxide liner 2210 also covers the horizontal surfaces at the trench edges. The result of performing this step is shown in FIGURE 22.

[0045] Then a layer of polysilicon 2310 is deposited using a low pressure chemical vapor deposition (LPCVD) process. The result of performing the LPCVD process to deposit the polysilicon 2310 is

shown in FIGURE 23. The two trenches are filled with polysilicon material 2310.

[0046] Then a polysilicon etchback process is performed to etch away the top layer of the polysilicon 2310. The result of performing the polysilicon etchback process is shown in FIGURE 24. Unlike the prior art polysilicon etchback process that has been previously described, the polysilicon etchback process of the present invention does not etch the polysilicon 2310 all the way down to the monocrystalline silicon substrate layer 1410.

[0047] The polysilicon etchback process of the present invention leaves a portion of polysilicon 2310 on top of each polysilicon filled trench. The portion of polysilicon 2310 that is located over the top of each polysilicon filled trench extends laterally over the edges of the trench in a shape that suggests the form of a nailhead. For this reason the portion of polysilicon 2310 that is located over the top of each polysilicon filled trench will be referred to as a polysilicon nailhead 2410. The initial height of silicon dioxide layer 1510 and the overetch height of the polysilicon 2310 are optimized to establish an appropriate height for the polysilicon nailhead 2410. The height of polysilicon nailhead 2410 must be sufficient for the polysilicon nailhead 2410 to survive subsequent etches and oxidations.

[0048] Then the silicon dioxide layer 1510 is stripped away. The result of stripping away silicon dioxide layer 1510 is shown in FIGURE 25. The polysilicon nailhead 2410 protects the silicon dioxide liner 2210.

[0049] During subsequent oxidations the silicon dioxide liner 2210 located between the polysilicon 2310 in the trenches and the surrounding monocrystalline silicon substrate layer 1410 is protected. Consider a subsequent oxidation that creates silicon dioxide layer 2610. During the oxidation process the external surface of polysilicon nailhead 2410 is oxidized. But the oxidation process can not reach the protected silicon dioxide liner 2210. There is no increase in volume in the silicon dioxide liner 2210 because the oxidized polysilicon nailhead 2410 can expand laterally and vertically. Therefore, there is no stress due to volume increase of the silicon dioxide liner 2210. The absence of stress means that there will be no defects in the surrounding monocrystalline silicon substrate layer 1410.

[0050] FIGURE 27 illustrates a flow chart 2700 showing the steps of a first portion of an advantageous embodiment of the method of the present invention. The manufacture of isolation trench structure 1400 of the present invention begins by providing monocrystalline silicon substrate layer 1410 (step 2710). Then a thick silicon dioxide layer 1510 is applied to the top of the

monocrystalline silicon substrate layer 1410 (step 2720). Then a layer of photoresist 1610 is then applied on top of the silicon dioxide layer 1510 (step 2730). Then the photoresist 1610 is selectively exposed and developed from the trench area (step 2740). Then portions of the silicon dioxide layer 1510 are etched anisotropically in the trench areas (step 2750).

[0051] Then the photoresist 1610 is removed before the silicon trench etch procedure is applied (step 2760). Then the silicon trench etch procedure is performed (step 2770). Control then passes to step 2210 of FIGURE 28.

[0052] FIGURE 28 illustrates a flow chart 2800 showing the steps of a second portion of an advantageous embodiment of the method of the present invention. Control passes to step 2810 from step 2770 of FIGURE 27. Then portions of silicon dioxide layer 1510 are etched away to pull silicon dioxide layer 1510 back from the trench edge (step 2810). Then a silicon dioxide liner 2210 is grown on the monocrystalline silicon substrate layer 1410 (step 2820). The silicon dioxide liner 2210 covers the walls and bottom of the trenches and the horizontal surfaces at the trench edges.

[0053] Then a layer of polysilicon 2310 is deposited using a low pressure chemical vapor deposition (LPCVD) process (step 2830). Then a polysilicon etchback process is performed to etch away the top layer of the polysilicon 2310 (step 2840). Then the silicon

dioxide layer 1510 is stripped away leaving polysilicon nailhead structures 2410 exposed (step 2850). These steps form the trench isolation structure 1400 of the present invention.

[0054] Although the present invention has been described with an exemplary embodiment, various changes and modifications may be suggested to one skilled in the art. It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.